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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,778	12/28/2001	Hiroaki Tanaka	GNE463A	4276

466 7590 04/03/2007

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER

ERDEM, FAZLI

ART UNIT	PAPER NUMBER
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2826

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/028,778

Applicant(s)

TANAKA ET AL.

Examiner

Fazli Erdem

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2, 4, 6, 8-11 and 15-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6, 8, 16, 18, 19 and 21 is/are allowed.
- 6) ☒ Claim(s) 2, 4, 10, 15, 22-29, 33, 35-41, 43, 46, 49 and 52 is/are rejected.
- 7) ☒ Claim(s) 9, 11, 30-32, 34, 42, 44, 45, 47, 48, 50, 51 and 53 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

After further search and consideration this action is issued and made non-final.

Allowable Subject Matter

1. Claims 6, 8, 16, 18, 19, 21 allowed.
2. Claims 9, 11, 30, 31, 32, 34, 42, 44, 45, 47, 48, 50, 51, 53, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
3. The following is a statement of reasons for the indication of allowable subject matter:
Prior art failed to establish a three layer TiN, Ti and Al conductive layer with Al in the bottom layer or four layer TiN, Ti and Al layer where Al is based in the lower middle layer.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
2. Claims 2, 4, 10, 15, 22-29, 33, 35-41, 43, 46, 49 and 52 rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al. (6,661,476) in view of Shimada et al. (6,448,578).

Regarding Claim 2, Abe et al. disclose a liquid crystal display device where in Figs 2, 4, 7, 9 and 11 it is disclosed an active matrix addressing LCD device comprising: an active matrix substrate dielectric plate 1, thin-film transistors G having a transparent, (TFTs) arranged on the plate 1, and pixel electrodes 2 arranged on the plate; gate electrodes G/9, of the TFTs having a

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first multilevel conductive structure 8/9/10; scan lines 41a/41b connected to the corresponding gate electrodes and having the first multilevel conductive structure; common electrodes 130, formed on the plate to be opposite to corresponding ones of said pixel electrodes; and common lines formed on the plate to be connected to corresponding ones of said common electrodes. Abe et al. fail to disclose the first and second multi-level structure including a TiN at top, Al in the middle and Ti in the bottom and the required nitrogen concentration of 25% or more for the TiN layer. However, Shimada et al. disclose a thin film transistor and liquid crystal display device where in Fig. 1 it is disclose 3 sets of multi-layer structure 4c/4b/4a, 3c/3b/3a and 9c/9b/9a where TiN at top (4c,3c,9c), Al layer in the middle (4b, 3b, 9b) and Ti layer in the bottom (4a, 3a, 9a). Furthermore, in column 7, line 4-35, the required nitrogen concentration of higher than 25% is disclosed.

It would have been obvious to one of having ordinary skill in the art the time the invention was made to include the required multi-layer conductive structure in Abe et al. as taught by Shimada et al. in order to have a liquid crystal display device with less film peeling and superior adhesion as disclosed in abstract section of Shimada eal.

Regarding Claim 4, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 10, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

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Regarding Claim 15, in Fig1 of Shimada et al. TFTs comprises a gate insulating film 11 formed to cover the gate electrode, a semiconductor island 6, formed on the gate insulating film, a source electrode 7 formed on the island, a drain electrode 8 formed on the island to form a channel gap between the drain electrode and the source electrode.

Regarding Claim 17, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 20, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 22, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 23, in Figs. 2, 4, 7, 9 and 11, Abe et al. disclose common electrodes 130, formed on the plate to be opposite to corresponding ones of said pixel electrodes; and common lines formed on the plate to be connected to corresponding ones of said common electrodes.

Regarding Claim 24, in Fig. 1 of Shimada et al. pixel electrode 9c/9b/9a has a multiple layer.

Regarding Claim 25, in Fig. 1 of Shimada et al. pixel electrode 9c/9b/9a has a multiple layer.

Regarding Claim 26, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 27, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 28, in Fig1 of Shimada et al. TFTs comprises a gate insulating film 11 formed to cover the gate electrode, a semiconductor island 6, formed on the gate insulating film,

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a source electrode 7 formed on the island, a drain electrode 8 formed on the island to form a channel gap between the drain electrode and the source electrode.

Regarding Claim 29, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 33, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 35, in Fig. 1 of Shimada et al. source electrode 4 has 3 layers (4c/4b/4a) and drain electrode 8 has three layers (9c/9b/9a) and aluminum layer is the middle layer 4b/9b.

Regarding Claim 36, in Figs. 2, 4, 7, 9 and 11, Abe et al. disclose common electrodes 130, formed on the plate to be opposite to corresponding ones of said pixel electrodes; and common lines formed on the plate to be connected to corresponding ones of said common electrodes.

Regarding Claim 37, in Fig. 1 of Shimada et al. pixel electrode 9c/9b/9a has a multiple layer.

Regarding Claim 38, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 39, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 40, in Fig. 1 of Shimada et al., TiN film 9c is exposed from the second multilevel conductive structure at the terminal 1.

Regarding Claim 41, in Fig1 of Shimada et al. TFTs comprises a gate insulating film 11 formed to cover the gate electrode, a semiconductor island 6, formed on the gate insulating film, a source electrode 7 formed on the island, a drain electrode 8 formed on the island to form a channel gap between the drain electrode and the source electrode.

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Regarding Claim 43, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 46, in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 49 in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Regarding Claim 52 in Fig. 1 of Shimada et al., Al film is the middle layer 3c, 3b and 3a.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


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FE

March 26, 2007


SUE A. PURVIS
SUPERVISORY PATENT EXAMINER